Controls for collimator MD

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MD schedule:
W 42 (Oct 18th)  16 Hrs TT40
W 44 (Nov 2nd)   24 Hrs LSS5
W 45 (Nov 9th)   24 Hrs LSS5
W 46 (Nov 16th)  16 Hrs Reserve
Outline

LSS5 Test

- Collimator Hardware
- Controls Hardware
- Controls Software
- Dry runs
- Remains to be done

**Note:** TT40 Test will be based on same (moveable rack) system used for collimator tests and commissioning.
- Installation 16 October
- Logging facilities ok?
Collimator HW (LSS5)

LHC collimator prototype

- **Motors**
  - Lep type: (not strong enough if skew > 5 ~7 mm)?
    Option, replace two motors by final motors in case there is time for doing so. (RL)

- **Position sensors**
  - 4 resolvers (lep motors: demultiplied, LHC: direct)
  - 4 potentiometers (Not possible to replace with final LVDT’s)
  - 2 LVDT’s for gap measurement.

- **Thermometers**
  - 8 PT100 (note: twice as much as final collimator, but 2 of them are dead)
Controls Architecture

- **Control room software:**
  - Management of settings (LSA)
  - Preparation for ramp
  - Assistance in collimator tuning
    - Based on standard LSA components
    - Dedicated graphical interface for collimator control and tuning

- **Collimator supervisor:**
  - Fesa Gateway to Control Room Software
  - Synchronization of movements
  - Beam Based Alignment
    - Support building, VME
    - Takes action on position errors (FB)
    - Receives timing, send sync signals over fiber to low level (ramp & Alignment)
    - Environmental Supervision
    - Communication with BLM using UDP

- **Low level control systems**
  - Motor drive
  - Position readout and survey
  - Environment Survey
    - Down stairs, PLC/VME/PIX?
    - 3 distinct systems / combined?
Controls Hardware

Low Level:
- PXI system (National Instruments, Labview-RT)
  Compact and cost effective solution
  Dedicated ACQ card for position readout, dedicated FPGA card for control
- PLC for temperature readout

Supervisor Level:
- PC gateway with timing receiver (Runs Fesa Server of the CSS and the Low Level Fesa Server)

Control Room Level:
- Terminal Servers, CCC console

BLM system (for LHC BLM’s):
- 4 LHC type (ionisation chambers) 10 downstream from collimators
- New FPGA based hardware with special option for short transient history readout.
Controls Hardware

Communication

- PXI system – Fesa Server
  - Dim (aka DIP), Ethernet
- Low Level (Fesa) - CSS (Fesa)
  - CMW, Internal
- CSS – PXI Synchronisation:
  - optical fibers (CTRP – CTDPR – CTDET)
- CSS – CCC app
  - CMW, Ethernet
- CSS – BLM (synchronised readout for beam based optimisation)
  - Synchronisation: Coax (ctrp – ctrp)
  - Data: UDP, Ethernet
Controls Software

What functionality will be available for the beam test:

- Basic command-driven control of single collimators for SPS test, TT40 test and commissioning of transfer line collimators.
- No function driven controls (March 2007)
- No BLM based alignment (August 2007)
- For PLC readout, display and logging: use standard system provided by Ph. Gayet.
Dry runs

Objectives:
• Test and validate the system long enough before the actual MD’s
• Provide a test bed to further validate and develop the system

Agenda:
• Thu 28 Sep: Validate architecture and communication
• Thu 5 Oct: Repeat, detailed evaluation
• Thu 12 Oct: Test with BLM synch/comm, PLC readout
• Tue 17 Oct: Validate system with real PXI hardware. Test Logging.
• Thu 19 Oct: Validate system with collimator in the lab.
• Thu 26 Oct: Validate system in BA5
Dry run Thu 28 September

Important step:
- Validation of basic architecture and communication (PXI - CSS - CCC_application, all except PCI hardware modules which were emulated in PXI)

It worked!
- We are now sure that there are no show stoppers or last minute problems in the whole communication chain.
- We learned what and where to improve.
- We can use the current system to further develop.

However, embedded controls in hardware modules still to be validated.
To be done

• HW installation
  – Installation of gateway
  – Connection with BLM
  – Connection CSS with Low Level
  – and not to forget TT40
• Test low level control (FPGA) and acquisition modules
• Integrate BLM transient recording
• Acquisition by subscription instead of polling.
• CCC application running from standard consoles
• Integrate with LSA environment
• Test logging of measurements and controls
• Validate temperature readout, display and logging
• Define access to calibration constants (offset and mm/step) for system initialisation.