

# Collimation MD

## Controls performance

# Collimator Controls Review

**18 December 13h30 – 17h00, 874-1-011**

- Introduction (Ralph Assmann) 10 min
- Lessons from the SPS controls test: (4 x ~20 min)  
Including the analysis of performance and faults.
  - External systems, temperatures and overall Architecture (M.Jonker)  
Logging, interface with BLM, Fesa, CMW, ...
  - Low Level: (R.Losito)  
(Motors, Resolvers, LVDT's, Motor Drivers, PXI system and software).
  - Middle Level: Collimator Supervisory System (CSS) (M.Sobczak)
  - Top level: Collimator control application for CCC (S.Redaeli)
- Break 20 min
- Issues for final controls system implementation
  - PXI or alternative options (R.Losito) 25 min
  - Architectural issues (M.Jonker) 15 min
  - Integration into machine protection (R.Assmann) 15 min
  - Integration into LSA (S.Redaeli) 15 min
- Proposed solution (M.Jonker/R.Assmann) 20 min

# Collimation MD

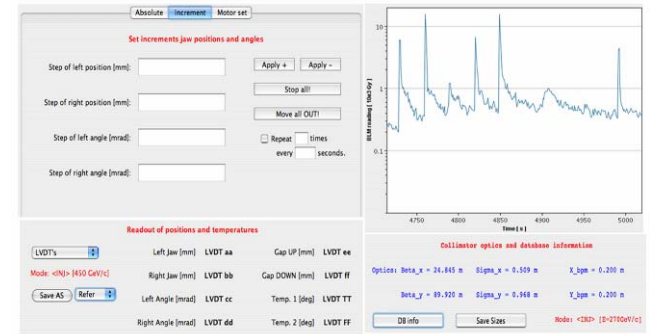
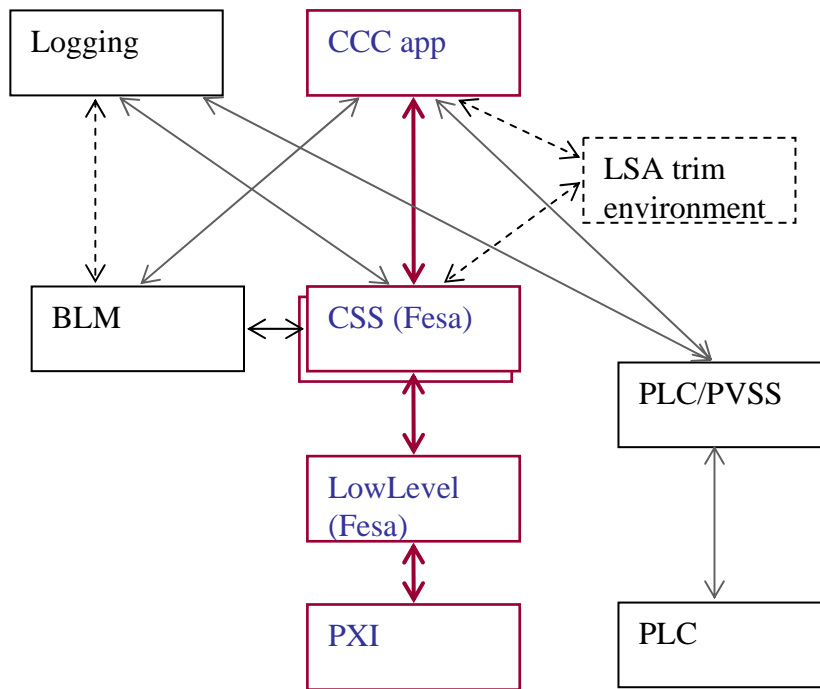
## LSS5 MD's 2 x 24 Hrs

- Week 44 31/10 – 01/11
- Week 45 07/11 – 08/11
- Parasitic MD (BLM transients 15/11)

## Objectives (From controls point of view)

- Commissioning of controls
- Validation of basic architecture and communication (**PXI** - CSS - CCC\_application)
- Test system performance
- Test synchronisation and communication with BLM

# Architecture



# Results

## It was a success

- Satisfactory performance of the control system.
- Many thanks to all those involved

8:00 to 15:00 Setup of low level

- treatment of noise on switch signal
- interlock signal disconnected and faked, reconnected afterwards
- Test of switches
- Calibration of LVDT signals

Control system up and running with an acceptable availability during the MD.

# What worked ?

- Full system was deployed (four layers)
- Able to control motors and readout positions through the entire chain.
- Collimator temperature readout.
- All data was recorded on logging database (as well as in private diagnostics acquisition files).
- Connection with BLM system worked (trigger and BLM transient results)

# What did we test

Test L/R/U/D coherency from high level interface

(motor - switches - lvdt's - resolvers)

Test calibration using repeated steps

(gap lvdt useless, potentiometers noisy bad)

Test mechanical play

up to 0.4 mm (dependent on position)

Test Transient BLM data

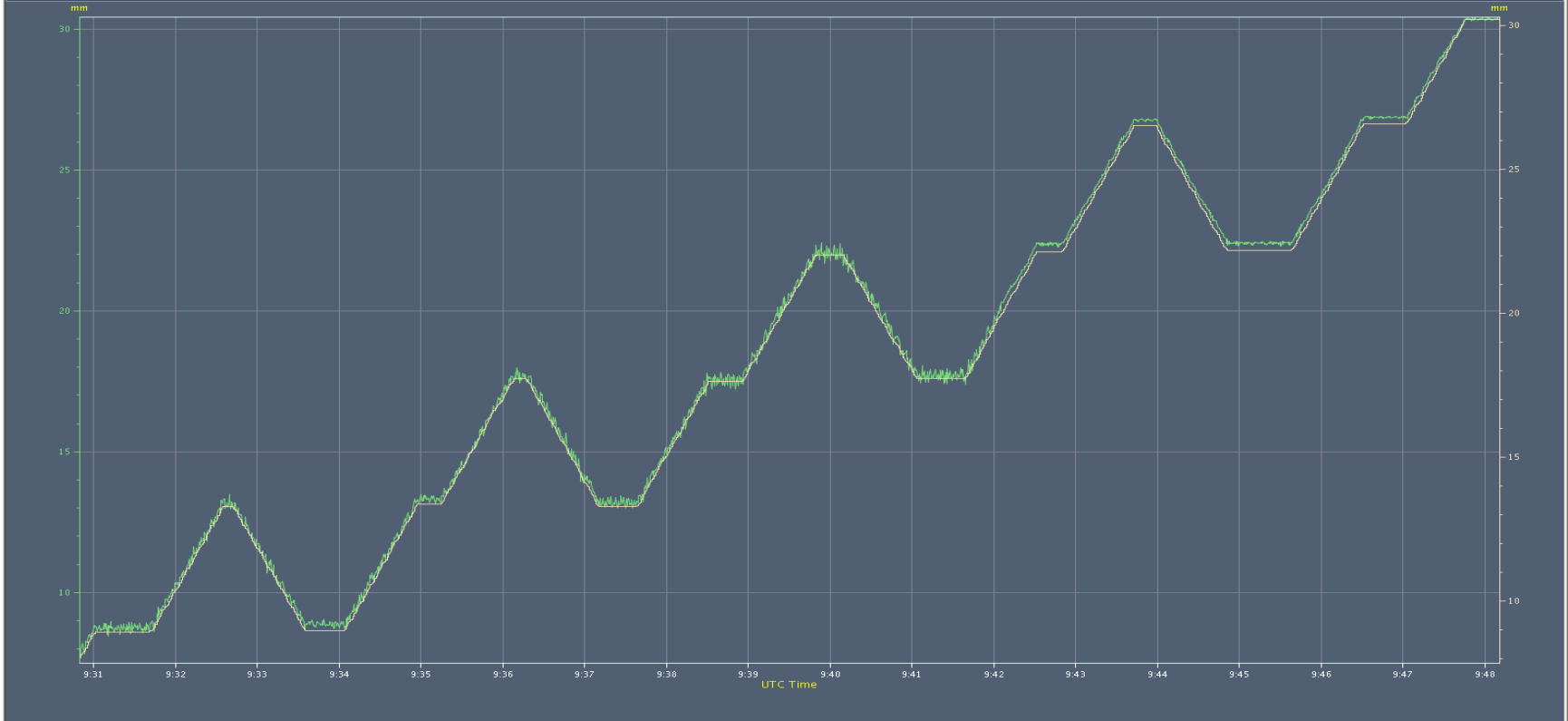
(not conclusive during the first two md's, results of the last md to be analysed in detail)

Not tested: left/right upstream/downstream with beam. (no prepared knobs)

Performance (repeat mode)

No crashes stressing the system to the limit (1000 repeated 5 um, 100 ms)

Response time: trigger to acknowledge for 20um step: ~40 ms (M.Sobczak)



Highlight not available for the Active Data Set at this zoom level.



# Problems encountered

## Hardware problems

- Motor induced noise on switch signals. Required installation of filters to correct.  
Note: LSS5 cable configuration is not the same as for the LHC!
- Poor resolution of Potentiometers (known)
- Gap LVDT's useless (known)
- Mechanical Play (known)
- One out of 6 temperature sensors sensitive to RF noise. (not LHC layout)

# Problems encountered

## **Structural problems:**

- System hanging with many ‘phantom’ TCP/IP connections (cmw) to error popup window on expert interface. We were surprised to see the system so gourmand in terms of TCP/IP connections
- Corba name server /CMW directory server went down, not possible to establish connections.  
  
System restart to be done in precise order
- Hanging of controls application (Java / CMW notification bug?) Still to be resolved

# Problems encountered

## **Performance problems:**

- Motor loosing steps not recognized.
- Time stamping of low level data out of step. (analysis by S.Redaeli)
- Poor resolution of LVDT's (Potentiometers)
- Mechanical Play
- One temperature sensor sensitive to RF noise.

# Future

Need a permanent controls test bed

## **Building 252:**

- Development of low-level system and CSS

## **Installed Collimators in transferlines T18:**

- Test and development of CSS and CCC application.

Improvements in architecture and in work organisation (specification, avoiding last minute implementations).